REMARKS

Status of the Claim

Claims 1-12, 18, 19 were previously cancelled.

Claims 13-17, 20 and 21 have been rejected.

By this response, **claims 13, 20, 21 have been amended**, and **claims 22, 23, 24 have been added.**

Response to Examiner's Office Action.

The Examiner rejected claims 13, 15-17, 20 and 21 under 35USC102(ab) as being anticipated by Christeson U.S. No. 6,622,243.

The Examiner stated;

"As per claim 13, Figure 1 of Christeson is directed to a memory back-up system comprising: a volatile memory cell (101); a non-volatile cell (102) that is interfaced with the volatile memory cell; a common control line (104) connected to the volatile memory cell and the non-volatile memory cell, the control line allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell (col. 3, lines 21-29).

Amended claim 13 includes the following features:

a volatile memory cell;

a non-volatile memory cell, the non-volatile memory cell being integrated with the volatile memory cell, the non-volatile memory cell being interfaced with the volatile memory cell;

a common control line connected to the integrated volatile memory cell and the non-volatile memory cell, the common control line allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell.
(Emphasis Added)

Support for the amendment of claim 13 can be found throughout the specification. For example, as stated on pages 6, 7 of the specifications "As shown in the drawings for purposes of illustration, the invention is embodied in an apparatus and a method for integrating volatile and non-volatile memory. The memory system allows for efficient transfer of large amounts of data between the volatile and non-volatile memory.

Figure 3 shows an embodiment of the invention. This embodiment includes a shared DRAM/MRAM memory cell 300 that includes a first memory cell 310, and a non-volatile memory cell 320 that is interfaced to the first memory cell 310."

Further, as stated on page 9 of the specification "The shared MRAM/DRAM memory cell 300 provides for the integration of MRAM and DRAM memory cells on a common substrate. As will be shown later, the integrated memory cell allows for the formation of integrated memory cell arrays in which large amounts of data can be easily transferred from MRAM cells to DRAM cells, and/or from DRAM cells to MRAM cells."

Figures 5, 6A, 6B, 6C, 6D, 6E show how to fabricate an embodiment of the integrated memory. Figure 5 shows a physical implementation of an MRAM/DRAM memory cell. Figures 6A, 6B, 6C, 6D, 6E show a process that can be used for forming the embodiment of Figure 5.

The courts have ruled that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. "Verdegall Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Also, "The identical invention must be shown in

as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The embodiments of Christeson include a processor 100, CMOS memory 101, and a non-volatile memory 102. The components communicate with each other over bus 104. The non-volatile memory preferable is flash memory. (Col. 2, lines 31-48).

Christeson does not provide features of the claimed invention. More specifically, Christeson does not provide non-volatile memory cell being integrated with the volatile memory cell. Additionally, Christeson does not provide a common control line connected to the integrated volatile memory cell and the non-volatile memory cell, the common control line allowing data to be simultaneously written to the volatile memory cell and the non-volatile memory cell.

Figure 1 clearly shows the CMOS memory and the non-volatile flash memory as two separate pieces of memory. The two separate pieces of memory require a data bus 104 for transferring data between the two separate pieces of memory. Christenson does not teach, describe or even suggest the desirability of integrating the non-volatile and volatile memory cells. The integration of the two types of memory allows a large amount of data to be transferred between the two types of memory efficiently (see applicant's specification page 14, lines 13-16).

Christenson teaches a preferred embodiment (Col. 3, lines 21-26) that includes an exit and same routine that further include computer-executable instructions, which cause new configuration information to be automatically stored in non-volatile memory 102 at the same time it is written into CMOS memory. Christenson clearly states that it is the computer-executable instructions which cause the configuration information to be written to both memory types at the same time. There is no way that computer-executable instructions can be construed to teach integration of the two types of memory, or a control line common to the two types of memory. There is absolutely no requirement that computer-executable instructions causing information to be written to two types of memory have common control lines.

Christenson shows a data bus 104 connecting the CMOS memory 101 and the Non-volatile memory 102. A data bus 104 is used to distribute data between devices. Data buses are not used for controlling memory or devices connected to the data bus. There is absolutely no discussion by Christenson regarding the controls for reading or writing data to the CMOS memory or the Non-volatile memory. Therefore, there is no way to conclude that control lines are shared between the two types of memory. The memory types suggested by Christenson include CMOS memory and flash memory. There is no suggestions whatsoever of using common controls for the CMOS memory and the flash memory.

Regarding claim 15, the Examiner stated:

> "Christenson is silent to disclose further comprising a second control line which in combination with the common control line provides selection of the volatile memory cell. However, this feature is seen to be an inherent teaching of the device since a means for providing a process of the system is disclosed and it is apparent that some type of control lines such as a control word line or control column must be present to select the volatile memory cell for the system to function as intended. For example, Christenson in column 2, lines 45-47 discloses that the volatile memory cell is a random access memory device, whose memory cell location needs the control word line and control column line to select the memory cell location as being understood by those skilled in the art."

Applicants respectfully disagree with the Examiner's rejection of claim 15. Claim 15 is dependent on claim 13 and should therefore be allowed. However, as explained above, there is no suggestion by Christenson to provide a common control line. Therefore, there is no way that Christenson suggests a second control line which in combination with the common control line provides selection of the volatile memory cell, because Christenson provides no suggestion of a common control line.

Regarding claim 16, the Examiner stated:

"Christenson is silent to disclose further comprising a third control line which in combination with the common control line provides selection of the non-volatile memory cell. However, this feature is seen to be an inherent teaching of the device since a means for providing a process of the system is disclosed and it is apparent that some type of control lines such as a control word line or control column must be present to select the volatile memory cell for the system to function as intended. For example, Christenson in column 2, lines 48 discloses that the non-volatile memory cell is a flash memory device, whose memory cell location needs the control word line and control column line to select the memory cell location as being understood by those skilled in the art."

Applicants respectfully disagree with the Examiner's rejection of claim 16. Claim 16 is dependent on claim 13 and should therefore be allowed. However, as explained above, there is no suggestion by Christenson to provide a common control line. Therefore, there is no way that Christenson suggests a third control line which in combination with the common control line provides selection of the volatile memory cell, because Christenson provides no suggestion of a common control line.

Claims 17, 20, 21 were rejected for the same reason as set forth in claims 13, 15 and 16.

Claims 17 is dependent on claim 13. Therefore, claim 17 should be allowed. Independent claims 20, 21 include the same features as claim 13. Therefore, claims 20 and 21 should be allowed.

The Examiner has indicated the claim 14 is allowable.

New claims 22, 23 include the following additional features:

*wherein a single word line WL is connected to both the first memory cell and the non-volatile memory cell.

*wherein the single word line WL is connected to a DRAM controlling transistor gate of the DRAM memory cell and a to a MRAM controlling transistor gate of the MRAM memory cell.

These additional features include additional details of one example of how the control lines of the invention can implemented.

New claim 24 includes the features of old claim 13 and 14. The Examiner indicated that this combination is allowable.

No new matter has been added by these amendments.

CONCLUSION

For the reasons given above, and after careful review of all the cited references, Applicant respectfully submits that none of the cited references, nor any combination of the cited references, will result in, teach or suggest Applicant's Claimed invention. But even if any such combination might arguably result in such Claimed invention, it is submitted that such combination would be non-obvious and patentable.

In view of the above Amendments and Remarks, Applicant has addressed all issues raised in the Office Action dated September 01, 2004, and respectfully solicits a Notice of Allowance for Claims 13-17, 20-24. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

It is believed that all of the pending Claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending Claims (or other Claims) that have not been expressed. Finally nothing in this paper should be construed as an intent to concede any issue with regard to any Claim, except as specifically stated in this paper, and the amendment of any Claim does not necessarily signify concession of unpatentability of the Claim prior to its amendment.

Applicant believes that no fees are currently due; however, should any fee be deemed necessary in connection with this Amendment and Response, the Commissioner is authorized to charge deposit account 08-2025, referencing the Attorney docket number 100201070-6.

Respectfully submitted,
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